

REMARKS

In view of the above amendments and the following remarks, reconsideration and further examination are respectfully requested.

I. Amendments to the Claims

Claims 1-10 have been amended to clarify features of the invention recited therein and to further distinguish the present invention from the references relied upon in the rejections discussed below.

II. 35 U.S.C. § 103(a) Rejection of Claims 1-4 and 8-10

Claims 1-4 and 8-10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Lee (U.S. 2001/0025976), Nam (U.S. 2003/0057464) and Takenaka (U.S. 6,339,008). This rejection is believed clearly inapplicable to amended independent claim 1 and the claims that depend therefrom for the following reasons.

Amended independent claim 1 recites a memory device comprising a plurality of memory cells, each memory cell including a memory cell capacitor, and the plurality of memory cells being arranged in a matrix along a first direction and along a second direction that is perpendicular to the first direction. Further, claim 1 recites that each respective memory cell capacitor includes a lower electrode, such that the lower electrode of each respective memory cell capacitor is independent from the lower electrodes of other memory cell capacitors. In addition, claim 1 recites that each respective memory cell capacitor includes a ferroelectric layer,

and an upper electrode, wherein each respective upper electrode of each respective memory cell capacitor of the plurality of memory cells that are only arranged along the second direction forms a continuous plate electrode covering only the respective independent lower electrodes of each respective memory cell capacitor of the plurality of memory cells that are only arranged along the second direction. Finally, claim 1 recites that the width of each respective upper electrode in the first direction is narrower than the width of each respective ferroelectric layer in the first direction. Lee, Nam and Takenaka, or any combination thereof fails to disclose or suggest the above-mentioned distinguishing features as recited in independent claim 1.

Rather, Lee merely teaches a capacitor that includes a second conductive film pattern 53 (lower electrode), a high dielectric film 55 (ferroelectric layer), and a third conductive film pattern 57 (upper electrode) (see Fig. 5 and paragraph [0050]).

Thus, in view of the above, it is clear that Lee merely teaches that an upper electrode 57 and a ferroelectric layer 55 are formed on a lower electrode 53, but fails to disclose or suggest that the width of each respective upper electrode in the first direction is narrower than the width of each respective ferroelectric layer in the first direction, as required by claim 1.

In other words, Lee cannot be relied upon for teaching that the width of each respective upper electrode in the first direction is narrower than the width of each respective ferroelectric layer in the first direction, as required by claim 1, because Lee fails to disclose or suggest any requirements for the widths of the third conductive film pattern 57 (upper electrode) and the high dielectric film 55 (ferroelectric layer).

Additionally, Applicants note that Figure 5 of Lee only appears to illustrate that the third

conductive film pattern 57 (upper electrode) has a thickness that is greater than a thickness of the high dielectric film 55 (ferroelectric layer) and that is greater than a thickness of the second conductive film pattern 53 (lower electrode). Thus, it is clear that Figure 5 of Lee does not suggest that the width of each respective upper electrode in the first direction is narrower than a width of each respective ferroelectric layer in the first direction, as required by claim 1.

Moreover, it is noted that Lee teaches that the third conductive film pattern 57 (upper electrode) is formed over the plurality of second conductive film patterns 53 (lower electrode) arranged along the first direction. Thus, it is clear that Lee fails to disclose or suggest each respective upper electrode of each respective memory cell capacitor of the plurality of memory cells that are only arranged along the second direction forms a continuous plate electrode covering only the respective independent lower electrodes of each respective memory cell capacitor of the plurality of memory cells that are only arranged along the second direction, as required by claim 1.

Now turning to Takenaka, Applicants note that Takenaka teaches that a capacitor includes an independent lower electrode 4, a ferroelectric film 8, and an upper electrode 9, wherein the upper electrode 9 is independent for each capacitor (see Fig. 1(e) and col. 6, lines 25-31 stating that the upper electrode 9 is patterned using a mask of the same size as the lower electrode 4). Applicants also note that electrode 9a of Fig. 1(d) is not the upper electrode 9 of the resulting capacitor.

Thus, in view of the above, it is evident that Takenaka teaches that that the lower electrode is independent for each capacitor and the upper electrode is the same size as the lower

electrode and is independent for each capacitor, but fails to disclose or suggest that the lower electrode of each respective memory cell capacitor is independent from the lower electrodes of other memory cell capacitors and that each respective upper electrode of each respective memory cell capacitor of the plurality of memory cells that are only arranged along the second direction forms a continuous plate electrode covering only the respective independent lower electrodes of each respective memory cell capacitor of the plurality of memory cells that are only arranged along the second direction, as required by claim 1.

Now, turning to Nam Applicants note that Nam merely teaches that a capacitor includes a lower electrode 216, a dielectric layer 218 and an upper electrode 220 (see Fig. 4), but fails to disclose or suggest that the width of each respective upper electrode in the first direction is narrower than a width of each respective ferroelectric layer in the first direction, as required by claim 1.

Moreover, Applicants note that Nam also teaches that a capacitor includes a lower electrode 316a, a dielectric layer 318a and an upper electrode 320a, wherein there is an independent upper electrode 320a for each capacitor (see Fig. 9), but fails to disclose or suggest that that the lower electrode of each respective memory cell capacitor is independent from the lower electrodes of other memory cell capacitors and that each respective upper electrode of each respective memory cell capacitor of the plurality of memory cells that are only arranged along the second direction forms a continuous plate electrode covering only the respective independent lower electrodes of each respective memory cell capacitor of the plurality of memory cells that are only arranged along the second direction, as required by claim 1.

Therefore, in view of the above-mentioned distinctions it is believed clear that independent claim 1 and claims 2-4 and 8-10 that depend therefrom would not have been obvious in view of the combination of Lee, Nam and Takenaka.

III. 35 U.S.C. § 103(a) Rejection of Independent Claim 5

Claim 5 was rejected under 35 U.S.C. § 103(a) as being unpatentable over various combinations of Lee, Nam and Yamada et al. (U.S. 2002/0096771). This rejection is believed clearly inapplicable to amended independent claim 5 and the claim that depends therefrom for the following reasons.

Independent claim 5 recites a memory device comprising a plurality of memory cells, each memory cell including a memory cell capacitor, and the plurality of memory cells being arranged in a matrix along a first direction and along a second direction that is perpendicular to the first direction. Further, claim 5 recites that each respective memory cell capacitor includes a lower electrode, such that the lower electrode of each respective memory cell capacitor is independent from the lower electrodes of other memory cell capacitors. Finally, claim 5 recites that a position of one edge along the second direction of each respective upper electrode substantially aligns with a position of one edge along the second direction of each respective ferroelectric layer, and that another edge along the second direction of each respective upper electrode is inwardly located at a position relative to another edge along the second direction of each respective ferroelectric layer. Lee, Nam and Yamada, or any combination thereof fails to

disclose or suggest the above-mentioned distinguishing features as recited in independent claim 5.

For reasons similar to those discussed above regarding claim 1, it is respectfully submitted that Lee and Nam fail to disclose or suggest that that the lower electrode of each respective memory cell capacitor is independent from the lower electrodes of other memory cell capacitors and that each respective upper electrode of each respective memory cell capacitor of the plurality of memory cells that are only arranged along the second direction forms a continuous plate electrode covering only the respective independent lower electrodes of each respective memory cell capacitor of the plurality of memory cells that are only arranged along the second direction, as required by claim 5.

Now turning to Yamada, Applicants note that Yamada teaches that a lower electrode 9 is a common electrode for two capacitors and that two upper electrodes 11 are separately provided on the ferroelectric film, such that each capacitor has an independent upper electrode 11 (see Fig. 1).

Thus, in view of the above, it is apparent that Yamada teaches that each capacitor has an independent upper electrode and that two capacitors share a common lower electrode, but fails to disclose or suggest that the lower electrode of each respective memory cell capacitor is independent from the lower electrodes of other memory cell capacitors and that each respective upper electrode of each respective memory cell capacitor of the plurality of memory cells that are only arranged along the second direction forms a continuous plate electrode covering only the respective independent lower electrodes of each respective memory cell capacitor of the

plurality of memory cells that are only arranged along the second direction, as required by claim 5.

Additionally, it is also noted that Lee, Nam and Yamada also fail to disclose or suggest that a position of one edge along the second direction of each respective upper electrode substantially aligns with a position of one edge along the second direction of each respective ferroelectric layer, and that another edge along the second direction of each respective upper electrode is inwardly located at a position relative to another edge along the second direction of each respective ferroelectric layer, as recited in claim 5.

Therefore, because of the above-mentioned distinctions it is believed clear that independent claim 5 and claim 6 that depends therefrom would not have been obvious in view of the combination of Lee, Nam and Yamada.

IV. 35 U.S.C. § 103(a) Rejection of Claims 6 and 7

Claims 6 and 7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over various combinations of Lee, Nam Yamada and Ohno (U.S. 5,923,062). This rejection is believed clearly inapplicable to amended independent claim 7 for the following reasons.

Independent claim 7 recites a memory device comprising a plurality of memory cells, each memory cell including a memory cell capacitor, and the plurality of memory cells being arranged in a matrix along a first direction and along a second direction that is perpendicular to the first direction. Further, claim 7 recites that each respective memory cell capacitor includes a lower electrode, such that the lower electrode of each respective memory cell capacitor is

independent from the lower electrodes of other memory cell capacitors.

Finally, claim 7 recites that a position of one edge along the second direction of each respective upper electrode substantially aligns with a position of one edge along the second direction of each respective ferroelectric layer, that another edge along the second direction of each respective upper electrode is inwardly located at a position relative to another edge along the second direction of each respective ferroelectric layer, and that one edge along the second direction of each respective independent lower electrode is inwardly located at a position relative to one edge along the second direction of each respective ferroelectric layer, and a position of another edge along the second direction of each respective independent lower electrode substantially aligns with a position of another edge along the second position of each respective ferroelectric layer.

For reasons similar to those discussed above regarding claim 5, it is respectfully submitted that Lee, Nam and Yamada fail to disclose or suggest that that the lower electrode of each respective memory cell capacitor is independent from the lower electrodes of other memory cell capacitors and that each respective upper electrode of each respective memory cell capacitor of the plurality of memory cells that are only arranged along the second direction forms a continuous plate electrode covering only the respective independent lower electrodes of each respective memory cell capacitor of the plurality of memory cells that are only arranged along the second direction, as required by claim 7.

Now turning to Ohno, Applicants note that Ohno teaches that a capacitor dielectric film 315 covers both edges of a high-layer electrode 313a, wherein an edge of the capacitor dielectric

film 315 is not disclosed (see Fig. 4G).

Thus, in view of the above, it is submitted that Ohno fails to disclose or suggest one edge along the second direction of each respective upper electrode substantially aligns with a position of one edge along the second direction of each respective ferroelectric layer, that another edge along the second direction of each respective upper electrode is inwardly located at a position relative to another edge along the second direction of each respective ferroelectric layer, and that one edge along the second direction of each respective independent lower electrode is inwardly located at a position relative to one edge along the second direction of each respective ferroelectric layer, and a position of another edge along the second direction of each respective independent lower electrode substantially aligns with a position of another edge along the second position of each respective ferroelectric layer, as recited in claim 7.

Therefore, because of the above-mentioned distinctions it is believed clear that independent claim 7 would not have been obvious in view of any combination of Lee, Nam, Yamada and Ohno.

VI. Conclusion

There is no disclosure or suggestion in Lee, Nam, Takenaka, Yamada and/or Ohno, or elsewhere in the prior art of record which would have caused a person of ordinary skill in the art to modify Lee, Nam, Takenaka, Yamada and/or Ohno to obtain the invention of independent claims 1, 5 and 7. Accordingly, it is respectfully submitted that independent claims 1, 5 and 7 and claims 2-4, 6 and 8-10 that depend therefrom are clearly allowable over the prior art of

record.

In view of the above amendments and remarks, it is submitted that the present application is now in condition for allowance and an early notification thereof is earnestly requested. The Examiner is invited to contact the undersigned by telephone to resolve any remaining issues

Respectfully submitted,

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